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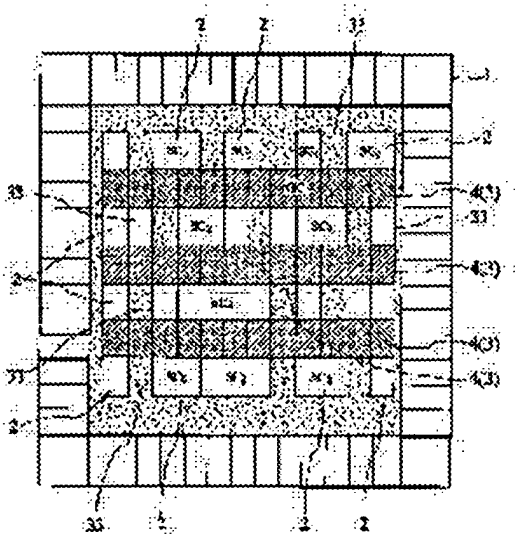
(54) INTEGRATED CIRCUIT AFTER STANDARD CELL SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain an integrated circuit which can be designed and manufactured in a short time by a method wherein a circuit can be changed without changing a gate polysilicon region or a source-drain region at the lower layer than the wiring layer of a standard cell.

SOLUTION: A plurality of standard cell arrays and fundamental cells GC used for a gate array are mounted on an identical chip 1 so as to be mixed. The fundamental cells GC which are used for the gate array are arranged in vacant regions 3 to be used as wiring regions between the plurality of standard cell arrays or in vacant regions 33 between the standard cells and the standard cells in identical standard cell arrays. Wiring layers are formed on the fundamental cells GC arranged as a spare cells so as to deal with a request for a circuit change.



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CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

* NOTICES *

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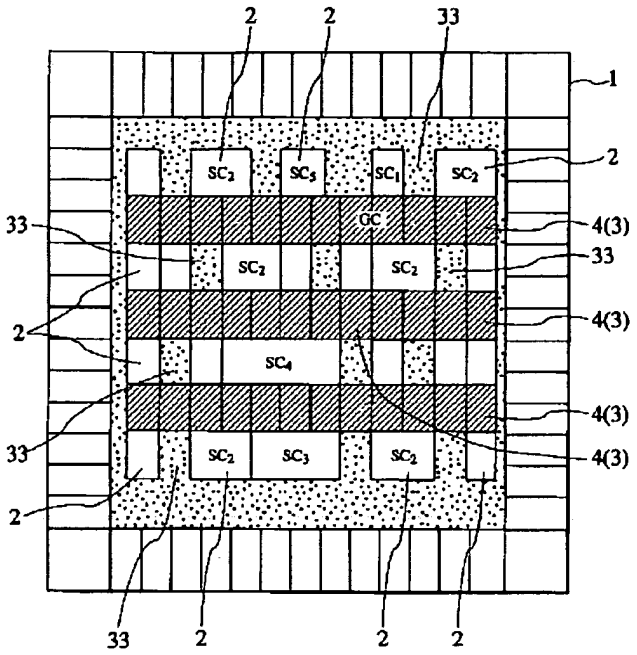
CLAIMS

[Claim(s)]
[Claim 1] The integrated circuit of the standard cell characterized by consisting of primitive cells of the gate array formed in the free area of the standard cell in a cel line predetermined [in two or more cel lines by which two or more standard cells were arranged, and these two or more cel lines] at least.
[Claim 2] Each of said standard cell is the integrated circuit of the standard cell according to claim 1 which is based on fixed height and the rectangle pattern space which has predetermined width of face, and is characterized by being based on predetermined width of face, the height of said standard cell, and a rectangle pattern space substantially with the same height by said primitive cell.
[Claim 3] The integrated circuit of the standard cell according to claim 1 characterized by having the primitive cell of the gate array formed in the wiring field arranged between each of two or more of said cel lines.
[Claim 4] The primitive cell formed in said wiring field is the integrated circuit of the standard cell according to claim 3 characterized by being based on a rectangle pattern space with the same height as predetermined width of face and the height of said standard cell.
[Claim 5] The integrated circuit of the standard cell according to claim 1 or 3 which said standard cell and said primitive cell adjoin in the direction which intersects perpendicularly with said cel line, and is arranged and is characterized by the standard cell which this adjoined, and a primitive cell having the common signal line of each other.
[Claim 6] Said standard cell and said primitive cell are the integrated circuit of the standard cell according to claim 1 or 2 characterized by having common power-source wiring arranged on a flat-surface layout at the same height.
[Claim 7] The width of face of said standard cell is the integrated circuit of the standard cell according to claim 1 to 6 characterized by being the width of face of the integral multiple of the width of face of said primitive cell.
[Claim 8] Said standard cell and said primitive cell are the integrated circuit of the standard cell according to claim 1 to 6 characterized by being arranged according to the same grid system.
[Claim 9] The integrated circuit of the standard cell characterized by forming the logical circuit field which has at least the primitive cell of the gate array formed in the free area of the standard cell in a cel line predetermined [in either / at least / a mega cell or a megger function two or more cel lines by which two or more standard cells were arranged, and these two or more cel lines] on the same semi-conductor substrate.
[Claim 10] Said logical circuit field is the integrated circuit of the standard cell according to claim 9 characterized by having further the primitive cell of the gate array formed in the wiring field between said two or more cel lines.

[Translation done.]

Drawing selection Representative drawing



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the integrated circuit of the standard cell which loaded together the primitive cell of a gate array in the circuit built by the standard cell.
[0002]
[Description of the Prior Art] Although the full custom IC is suitable when manufacturing high performance IC in large quantities, it has the fault that the period from a design to manufacture is long. On the other hand, semicustom IC is suitable, when developing LSI which a user wishes for a short period of time by performing patterns, such as a logic cell of the interior, by the design automation by the computer. Also in the full custom-made design, although the design automation by the computer may be taken in, automation is applied mainly to prediction of circuit actuation, and verification of a pattern in this case. In other parts of a design, a standardization of design automation is not made but the design technique which borrowed the assistance of the so-called computer which a designer performs interactively is taken in.
[0003] On the other hand, the semi custom-made technique is the design automation by the computer by which the design technique was standardized, and the gate array method and the standard cell are known. The gate array method has the features that LSI in alignment with a user's hope can be developed for a short period of time, by having created beforehand the master chip which arranged the primitive cell in the shape of a grid, performing only the design of the metal wiring layer of the upper part of a primitive cell, and making only wiring connection of this metal wiring layer. as the factor which a gate array can develop for a short period of time -- (**) --; whose production process is only a wiring process of a metal wiring layer -- (**) -- since LSI is designed and logic verification is performed by design automation (DA) using a cel [finishing /; (Ha) verification with the short period (preparation) of mounting and evaluation / since the number of chip size pads etc. was decided beforehand], the check of a function is prompt and it is raised that there is no trouble by mistake etc.
[0004] On the other hand, although the standard cell is similar to a gate array method at the point which is the method which realizes the integrated circuit to which a desired logical function is beforehand satisfy using the library of the cel design and verified by the help or the calculating machine, the cel use with this standard cell usually has the logical function of a simple logic gate or a flip-flop or the like, it is height H regularity and the rectangle pattern of width of face W geometrically, and width of face W has an adjustable configuration in many cases. As shown in drawing 16 , generally it is covered with such a standard cell (SC1, SC2, SC3, SC4, SC5, --) 100 all over a chip 101, and it is not arranged. That is, after the chip 101, the wiring field or free area 102 in which wiring for connecting between standard cells 100 is formed is prepared. The free area 102 by which this standard cell 100 is not arranged was used, only in order that functional devices, such as a transistor, might be left behind as a field which is not arranged at all and might only form wiring.
[0005] In the integrated circuit built using such a standard cell, when a design change is needed with circuit modification etc., if the number or structure of a transistor do not change temporarily, only

correction of wiring is required, but when an excessive transistor is required, additional arrangement of a transistor is newly needed. In this case, modification from a CVD process and a RIE process for more nearly alternative ion grouting for forming the diffusion layer of the source drain field which it becomes impossible to manage only with modification of wiring, and constitutes the process before a wiring process, i.e., a transistor, to form a polish recon layer was needed. Modification of the mask pattern naturally used for these processes also joins modification of these processes. For this reason, when circuit modification accompanied by additional arrangement of a transistor arose, the development cycle of LSI of a standard cell was long.

[0006] On the other hand, a gate array method is a method which builds a desired circuit by connecting the primitive cell arranged regularly on a matrix, and fixed. The primitive cell used by this method has simple logic cells, such as a thing, the simple gate which comes to connect 1 or two or more primitive cells, a flip-flop, etc. without a logical function, only by it. It was in the integrated circuit of such a gate array method, and especially in the thing called a whole surface **** stuffing mold, uniform transistor array was beforehand arranged all over the chip, and various circuits were built by using the part in it. Also in this gate array method, the transistor which is not used like a standard cell is left behind as it is. For this reason, when circuit modification arose, it was able to be coped with by modification of only wiring using these intact transistors. Moreover, by the gate array method, since the master slice prepared beforehand was used, the time necessary for completion requires only the design of only a wiring part, and was able to be developed in the short period. However, by the gate array method, since only the primitive cell currently prepared beforehand was used in designing a circuit, there was a fault that the degree of freedom of a circuit design -- size of a transistor cannot be made small -- was restricted.

[0007] Memory, a core based CPU, ALU, A/D, a D/A converter, and various I/O circuits also including a display are included, so that you may surely say a large-scale circuit system. Even if a circuit scale grows large, the need of naturally carrying such a subsystem in the same chip arises. Therefore, a memory logic mixed-loading technique, an analog-to-digital mixed-loading technique, etc. are becoming important recently. For this reason, the en BEDDEDDO array (embeded array) which made possible synchronization of manufacture of a substrate and the design of the gate array section has appeared combining a compound form [where the field only for memory was established in a part of master chip] gate array, a channel loess form gate array and a bulk memory as shown in drawing 17 , or a processor core on the same chip. Since about the same degree of integration and flexibility as a standard cell, and about the same development cycle compaction as a gate array are possible for this, it attracts attention recently. The case where the channel loess form gate array field 221 and the channel loess form standard cell field 222 are formed with a mega cell 213 and the megger function 211,212 on a chip 201 in drawing 17 is shown. Memory, such as ROM by which "a mega cell 213" has the fixed layout pattern of a cel, and the engine performance tends to be influenced by the layout, and RAM, or a multiplier is a typical cel. Although "the megger function 211,212" is logically treated as a cel of a lump, its ALU and core based CPU to which it realizes combining a macro cell and connection relation with other blocks tends to affect a chip degree of integration are [a layout top] typical. The channel loess form gate array field 221 is a field of the gate array which loses a wiring field, covers the whole surface with a gate array, and enabled it to use a primitive cell top for wiring and a functional cel if needed. Moreover, the channel loess form standard cell field 222 is a field which lost the wiring field and covered the whole surface with the standard cell.

[0008]

[Problem(s) to be Solved by the Invention] When circuit modification accompanied by additional arrangement of a transistor arose if it was in the integrated circuit of the conventional standard cell as explained above, modification of long "front process" of process time amount was needed also among all the processes that manufacture the integrated circuit of forming a source drain diffusion layer and a gate polish recon layer, and the fault that the development cycle of an integrated circuit became long as a result was caused. For example, although a wiring process is about 2 day room, as for "the front process" below a wiring layer including a diffusion process etc., spending more than for seven days is common.

[0009] If it is in the integrated circuit of the conventional gate array method, since a design change becomes possible only by modification of wiring on the other hand, while it has the advantage that a circuit change can be made easily, since the primitive cell which can be used is simple, the degree of freedom of a circuit design is low compared with a standard cell. For this reason, if it was in the integrated circuit of a gate array method, the fault of being generated also when it becomes difficult for that circuit design to carry out and to obtain the desired circuit engine performance in ****** was caused. For example, even if it was going to make power consumption of a specific circuit small, the size of a transistor is immobilization and it had the fault that the current beyond the need will flow.
[0010] These troubles of the en BEDDEDDO array shown in drawing 17 are also the same, cannot free themselves from the standard cell, and the original engine performance or original property of a gate array in the field 222 which covered the whole surface with the standard cell, and the field 221 which covered the whole surface with the gate array, either, and do not solve at all the original trouble which these conventional cels have.
[0011] Then, arrangement wiring of the cel on a chip and circuit modification are easy for the place which this invention is made in view of the above, and is made into that purpose, and are to offer the integrated circuit of the standard cell which can attain shortening of a development cycle.
[0012] It is that the more concrete purpose of this invention offers the integrated circuit of the standard cell which can be manufactured for a short period of time easily [modification of circuits, such as a change in the drive capacity of a circuit, and a change in the power consumption of a circuit,].
[0013]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, it is characterized [1st] by this invention being semicustom IC which has at least the primitive cell of the gate array formed in the free area of the standard cell in two or more cel lines and a cel line predetermined [in two or more of these cel lines]. Here, as for each cel line, it is needless to say respectively that two or more standard cells are arranged and constituted. And each standard cell is based on the rectangle pattern space which has the predetermined width of face W to fixed height H. That is, the appearance of a standard cell is carrying out the rectangle pattern configuration of X (height H) (width of face W). The width of face W of a rectangle pattern space is adjustable, and can take various values. Since wiring becomes easy to carry out the primitive cell of the gate array formed in the free area of a standard cell, it is desirable to be based on a rectangle pattern space substantially with the same height H with the predetermined width of face W and the height of a standard cell. It is the mind referred to as that the appearance of the primitive cell of a gate array is carrying out the rectangle pattern configuration of X (width of face W) (height H) except for the configuration of the transistor pattern of the interior etc. with "it is based on a rectangle pattern space." You may make it form the primitive cell of a gate array in the wiring field not only between the free area of a standard cell but further two or more cel lines. Moreover, the free area as a wiring field between two or more cel lines is deleted and each cel line may form the primitive cell of a gate array in the free area of the standard cell in a cel line predetermined [of them] in the channel loess form standard cell which adjoined mutually and has been arranged to make the degree of integration of an LSI chip high.
[0014] According to the 1st description of this invention, the primitive cell of a gate array is preparatorily arranged to the free area by which the standard cell is not arranged, and when the demand of circuit modification occurs, a circuit change can be made using this primitive cell. For this reason, various circuit modification is attained only by modification of the upper circuit pattern, without affecting "the lower layer pattern" of a standard cell. Since formation of the polish recon gate field below a wiring layer or a source drain field takes a long time overwhelmingly in the production process of LSI, the development cycle of an integrated circuit when a design change and specification modification arise can be sharply shortened by not changing the pattern of these lower layers. Moreover, by arranging a standard cell and a primitive cell by the same grid system, or doubling a predetermined design specification, such as doubling the height of both rectangle pattern, mixed loading of both to a semiconductor chip top can be made easy, and the constraint on arrangement / wiring can be sharply eased compared with the former.

[0015] The 2nd description of this invention starts a large-scale circuit system including memory, a core based CPU, ALU, A/D, a D/A converter, and various I/O circuits also including a display. That is, the 2nd description of this invention is having formed "the logical circuit field (logical block)" of the standard cell gate array mixed-loading form it having explained in the 1st description with either [at least] the mega cell or the megger function, on one LSI chip (semi-conductor substrate). The memory and the multipliers with which the layout pattern of a "mega cell" of a cel is fixed with multipliers, and the engine performance tends to be influenced by the layout, such as ROM and RAM, are typical cels here. Although a "megger function" is logically treated as a cel of a lump, its ALU and core based CPU to which it realizes combining a macro cell and connection relation with other blocks tends to affect a chip degree of integration are [a layout top] typical.
[0016] The LSI chip which formed the mega cell etc. and the logical circuit field on the same chip also conventionally is proposed. However, in this case, it is covered with all logical circuit fields by the standard cell, or was altogether covered with them by the primitive cell of a gate array. Therefore, by such large-scale circuit system, when specification modification and a design change occurred, a series of processes, such as pattern modification of a lower layer gate polish recon field or a source drain field, an ion implantation accompanying this, oxidation, and CVD, RIE, needed to be redone from the start, turn around time (TAT) became long, and a prompt action was not completed in the design change of an integrated circuit, and specification modification.
[0017] Since according to the 2nd description of this invention a circuit change can be made using this primitive cell when the primitive cell of a gate array is preparatorily arranged beforehand to the free area by which the standard cell of a logical circuit field is not arranged and specification modification and a design change arise, a circuit change can be made without affecting the circuitry of a standard cell. That is, it is not necessary to redo a lower layer ion grouting degree etc., various circuit modification is attained only by modification of the upper wiring, and the development cycle of an integrated circuit can be shortened. Moreover, the constraint on both arrangement wiring can be sharply eased compared with the former by doubling the base dimension of a standard cell and a primitive cell, or arranging these cels on the same grid.
[0018] Since the size of a transistor is immobilization, even if demand of wanting to make the transistor of the specific field on a chip small depending on a user's specification, and to make power consumption small produces especially the primitive cell of a gate array, modification of such size has the fault which is not made. On the other hand, since the size of the transistor in the inside of the cel field will be adjustable even if height H of a cel is immobilization, a standard cell can make size of a transistor small according to requirement specification, and can lower power consumption. Therefore, it is possible to lower the power consumption of the whole LSI chip by combining the primitive cell and standard cell of a gate array appropriately. That is, high integration and low-power-izing of a standard cell become possible [combining both the features that it is easy and a circuit design is rich in flexibility, and the features that the development cycle of a gate array is short] by loading together a standard cell and the primitive cell of a gate array to a logical circuit field (logical block). Arrangement of the middle buffer for furthermore controlling increase and the clock skew of drive capacity with the combination of a standard cell and the primitive cell of a gate array becomes easy. Thus, according to the 2nd description of this invention, an improvement of properties, such as the operation time of a large-scale LSI chip and power consumption, and the formation of a high accumulation consistency are easy, and, moreover, the flexible circuit design of them becomes possible. And it can respond promptly also to a design change and TAT becomes short.
[0019]
[Embodiment of the Invention]
[Gestalt of the 1st operation] drawing 1 is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 1st of this invention. A multi-line array is carried out on a chip 1, and the place by which it is characterized [of the gestalt of this 1st operation] has the cel line which consists of an array of a standard cell (SC1, SC2, SC3, SC4, SC5, --) 2 in having arranged preparatorily the primitive cell 4 used for the free area 3 which exists between each

of two or more of these cel lines by the gate array, as shown in drawing 1 . In such a configuration, the original circuit design is built by the standard cell 2. However, when circuit modification called correction and addition of a circuit is needed after that, correction and addition of a circuit are performed using the transistor in the primitive cell 4 of this gate array arranged preparatorily. In addition, you may make it use a primitive cell 4 from the phase of the beginning of a circuit design.

[0020] By such technique, since the pattern of these primitive cells can be used when the primitive cell 4 of the gate array beforehand arranged as a dummy is prepared and the need for circuit modification arises after that, various circuit modification becomes possible by modification of only the pattern of a wiring layer.

[0021] For this reason, circuit modification is attained simply, without making a lower layer pattern change of a source drain diffusion layer, a gate polish recon layer, etc., and performing processes, such as an ion implantation of the preceding paragraph story accompanying these, and CVD, RIE, like the conventional standard cell. Circuit modification generated later can be carried out for easy and a short period of time, without the size and the number of a transistor which are the advantage of a standard cell spoiling the degree of freedom of the circuit design of being able to choose it as arbitration by this. Moreover, mixed loading of a standard cell 2 and a primitive cell 4 is attained simply, without affecting the location and circuit engine performance of a standard cell 2 which replaced with the standard cell 2 and have arranged the primitive cell 4 at the beginning in the location where a standard cell 2 should be arranged essentially compared with the technique replaced and arranged, since he is trying to arrange a primitive cell 4 to the free area 3 of a standard cell 2.

[0022] In the case of drawing 1 , this invention is not restricted although drawing 1 arranges the primitive cell of a gate array only between a cel line and a cel line. Usually, the cel line of a standard cell has the free area 33 also in the cel line. Therefore, as shown in drawing 2 , a primitive cell may be further arranged also to the free area 33 between the standard cell 2 in each cel line, and a standard cell 2. Moreover, as shown in drawing 3 , a primitive cell may be arranged only to the free area 33 between a standard cell 2 and a standard cell 2. The configuration method of drawing 3 is more effective in drawing 4 which showed the flat-surface pattern of a standard cell **** stuffing form. Since there is no drawing 4 of three wiring channel field, an accumulation consistency becomes very high.

[0023] Thus, the primitive cell 4 arranged preparatorily is not only used for modification of a mere circuit specification, but in order to improve the property of a circuit more, it can use it. For example, since the middle buffer for distributing the clock signal from the clock driver 51 to the circuit constituted on the chip 1 is constituted, it can also be used. Although the circuit system of a tree structure etc. is used as generally shown in drawing 5 (a) in order to control the clock skew of a circuit, it depends for the time delay to a circuit end on arrangement of the standard cell which constitutes the circuit scale of tree each branch, and it. For this reason, before arrangement of a standard cell, very becomes difficult [prediction of a time delay], and the circuitry which distributes a clock signal is considered after arrangement of a standard cell, and is changed more often. In such a case, if the primitive cell 4 of a gate array is beforehand arranged to the free area 3 of a standard cell 2, it will become possible to constitute the middle buffers 52, 53, --, 58 and -- using this primitive cell 4 arranged beforehand, as shown in drawing 5 (b). Thereby, the middle buffers 52, 53, --, 58 for controlling clock skew and -- can consist of standard cells 2 easily, without changing the circuit arrangement till then constituted at the beginning.

[0024] Moreover, when drive capacity is insufficient or it becomes clear that a time delay is inadequate as a result of carrying out examination evaluation of the property of the circuit once the circuit was constituted by the standard cell 2, it can be immediately coped with by combining the primitive cell 4 of a standard cell 2 and a gate array. That is, it becomes possible to constitute easily a circuit with the optimal drive capacity or a time delay property only from pattern modification of a metal wiring layer, without changing the circuit built till then or adding a new standard cell.

[0025] the 1st example concerning the gestalt of operation of the 1st of the 1st example this invention -- drawing 3 R> -- in a configuration as shown in 3 or 4, the pattern layout at the time of making equal height H in the dimension (height H and width of face WS and WG) of a standard cell and a primitive cell (BASIC cel) is shown. That is, drawing 6 is the top view before forming the wiring layer in the

pattern layout at the time of making height H equal, and drawing 7 is a top view at the time of forming a metal wiring layer on drawing 6 , having used the location of a power supply terminal (power-source wiring) as the same. In drawing 7 , contiguity arrangement of the primitive cell (primitive cel) of the standard cell which constitutes the NAND (nonconjunction) gate 5 of 2 inputs using CMOS, and the gate array which constitutes an inverter 6 using CMOS is carried out. Here, a "primitive cel" means the cel in which the metal wiring layer was formed on the "BASIC cel", and although both are serially different patterns, they are the cels same as a pattern location on a chip. That is, although the vocabulary of the "BASIC cel" is used in drawing 6 and the vocabulary of a "primitive cel" is used in drawing 7 , both are the cels same on the real target stationed in the same location. However, the cel in which the metal wiring layer is not serially formed in addition in the next phase is still called the "BASIC cel." Drawing 8 is the equal circuit display of drawing 7 .

[0026] As shown in drawing 6 , in the 1st example concerning the gestalt of operation of the 1st of this invention, the n well 96 of a standard cell and the n well 98 of the primitive cell (BASIC cel) of a gate array overlap, and are arranged. Moreover, the p well 95 of a standard cell and the p well 97 of the primitive cell (BASIC cel) of a gate array overlap, and are formed. Namely, height H and width of face WG The primitive cell 6 of a gate array, height H, and width of face WS A standard cell 5 overlaps and is arranged. In the n well 96 of a standard cell, it is p+. Source field 75S and p+ Drain field 75D and n+ The contact field 77 is formed. In the p well 95 of a standard cell, it is n+. Source field 76S and n+ Drain field 76D and p+ The contact field 78 is formed. Furthermore ranging over the field of both the n well 96 and the p well 95, the common gate polish recon fields 64 and 65 are formed. On the other hand in the n well 98 of the primitive cell of a gate array, it is p+. Source field 71S and p+ Drain field 71D and n+ The contact field 73 and the gate polish recon field 61 are formed. In the p well 97 of the primitive cell of a gate array, it is n+. Source field 72S and n+ Drain field 72D and p+ The contact field 74 and the gate polish recon field 62 are formed.

[0027] As shown in drawing 7 , it is p+ of the primitive cell (primitive cel) of a gate array. p+ of source field 71S and a standard cell Source field 75S are connected to the high order power-source wiring (VDD) 9 prepared on the straight line of the same height on the flat-surface pattern through the contact hole 382,393,391. n+ of the primitive cell (primitive cel) of a gate array Source field 72S and n+ of a standard cell Source field 76S are connected to the lower order power-source wiring (VSS) 10 prepared on the straight line of the same height on the flat-surface pattern through the contact hole 386,397.

[0028] the inverter of the primitive cell (primitive cel) of a gate array -- pMOSFETQ1 nMOSFETQ2 from -- it is constituted. pMOSFETQ1 The polish recon gate electrode 61 and nMOSFETQ2 The wiring 351 which connects the polish recon gate electrode 62 of each other through a contact hole 383,384 constitutes the input terminal C of an inverter. pMOSFETQ1 p+ Drain field 71D and nMOSFETQ2 n+ The wiring 352 which connects drain field 72D mutually through a contact hole 381,385 serves as the output terminal X of an inverter.

[0029] two pMOSFETQ(s)3 by which parallel connection of the 2 input NAND which consists of standard cells is carried out to the high order power-source wiring (VDD) 9, and Q4 This pMOSFETQ3 and Q4 Common p+ Two nMOSFETQ(s)5 by which series connection was carried out between drain field 75D and the lower order power-source wiring (VSS) 10, and Q6 from -- it is constituted. pMOSFETQ3 nMOSFETQ5 The metal terminal 354 connected to the common gate polish recon field 64 through a contact hole 392 constitutes one input terminal A of the 2 input NAND. pMOSFETQ4 nMOSFETQ6 The metal terminal 355 connected to the common gate polish recon field 63 through a contact hole 399 constitutes the input terminal B of another side of the 2 input NAND. pMOSFETQ3 and Q4 Common p+ the drain field 75 -- D and nMOSFETQ5 n+ The wiring 353 which connects source field 76S mutually through a contact hole 395,398 constitutes the output terminal Y of the 2 input NAND.

[0030] In such a configuration, since the location of the height (H) of the dimension of each cel and the height direction of the high order power-source wiring (VDD) 9 and the lower order power-source wiring (VSS) 10 is designed identically Since it will be in the condition that the power-source wiring 9 and 10 of both cels is connected only by have arranged the primitive cell easily between standard cells,

and carrying out contiguity arrangement of both the cels, connection of power-source wiring can be performed easily. Moreover, it may be made to make the same the height of other signal wiring other than power-source wiring, and it becomes possible [connecting the signal wiring of both cels easily also in this case].

[0031] The 2nd example drawing 9 is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the 2nd example of the gestalt of operation of the 1st of this invention. As shown in drawing 9 , height is the same and the standard cells SC1-SC4 which are four kinds from which width of face differs are arranged on the semiconductor chip. The inside of the cel lines 13a and 13b by which standard cells SC1-SC4 were arranged the place by which it is characterized [of this 2nd example], and the free areas 14a and 14b between 13c, Height is at free-area 14a with the height more than the height (namely, height of the cel lines 13a, 13b, and 13c) of standard cells SC1-SC4 to have arranged alternatively primitive cell GC of the gate array designed identically to it of standard cells SC1-SC4. Furthermore, primitive cell GC of one gate array is loaded together by primitive cell GC of four gate arrays, and cel line 13c at cel line 13a at primitive cell GC of one gate array, and cel line 13b. These primitive cell GC is designed identically [the location of height, the high order power-source wiring (VDD) 11, and the lower order power-source wiring (VSS) 12] to it of standard cells SC1-SC4.

[0032] In addition, in drawing 9 , other signal wiring except the power-source wiring 11 and 12 is omitted. Even if it is in such 2nd example, the same effectiveness as the 1st example of the above can be acquired.

[0033] The 3rd example drawing 10 is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the 3rd example of the gestalt of operation of the 1st of this invention. The place by which it is characterized [of the 3rd example] as shown in drawing 10 has the same height, and height is at the cel lines 15a and 15b by which the standard cells SC1-SC5 which are five kinds from which width of face differs were arranged, and the free area 16 between 15c to have arranged primitive cell GC of the gate array designed identically to it of standard cells SC1-SC5. Furthermore, primitive cell GC of one gate array is loaded together by primitive cell GC of four gate arrays, and cel line 15c at cel line 15a at primitive cell GC of one gate array, and cel line 15b. The height of each of these cel lines 15a and 15b and primitive cell GC inserted and arranged in 15c, respectively is designed identically to it of standard cells SC1-SC4. Moreover, the location of the high order power-source wiring (VDD) 11 of each cel lines 15a and 15b and the primitive cell GC upper part inserted and arranged in 15c, respectively and the lower order power-source wiring (VSS) 12 is designed identically to it of standard cells SC1-SC4. At drawing 10 , it is the standard cell SC 11 of cel line 15b. It connects with a standard cell SC 4 through wiring s1, a standard cell SC 4 minds wiring s2, and it is a standard cell SC 12. It connects. Moreover, the standard cell SC 3 of cel line 15c minds wiring s5, and it is a standard cell SC 13. It connects and is a standard cell SC 13. It connects with the standard cell SC 2 through wiring s6.

[0034] In the design of a standard cell with the free area 16 of cel spacing as shown in drawing 10 , the height of the free area 16 of cel spacing or the height of a standard cell is adjustable. By the design approach of a standard cell, in order to perform the pattern design which met a user's hope from the beginning, the size of a transistor can be chosen freely and it has the description with easy optimization of wiring for connecting each standard cell. Since it has such a degree of freedom, generally the height of a standard cell is smaller than the primitive cell of a gate array. When the height of the primitive cell of a gate array is smaller than the height of the primitive cell of a general gate array, the difference in the height of a standard cell and the primitive cell of a gate array decreases, and even if it loads together and uses a primitive cell for a standard cell, the increment in area-decreases. For this reason, width of face is more smallish, as shown in drawing 7 , when it replaces with the primitive cell of a gate array, it arranged from the beginning and circuit modification arises, the number of a standard cell from which area becomes almost the same as the primitive cell of a gate array of the primitive cell which can be used for this circuit modification increases, and it becomes easy to change it. Thereby, when a design change arises on the way, it becomes possible to cope with it only by modification of the process after the process which forms a wiring layer, and the time amount spent on circuit modification can be

shortened. Moreover, if there are the cel trains 15a and 15b and a part where exchange of the standard cell in 15c is expected even if it is the last standard cell from which area would become the same as the primitive cell of a gate array, it replaces with a standard cell beforehand in this part expected, you may make it arrange primitive cell GC, and a change can be made easily even in this case.

[0035] In the 4th example [3rd] of the example above, reference was not made about the primitive cell train GC arranged at the free area 16 in the pattern layout shown in drawing 10 . Drawing 11 is drawing showing the example (the 4th example of the gestalt of operation of the 1st of this invention) which used the primitive cell train GC arranged at the free area 16, and made a circuit change by modification of the process after a wiring process. At drawing 10 explained in the 3rd example, it is the standard cell SC 11 of cel line 15b. It connects with a standard cell SC 4 through wiring s1, a standard cell SC 4 minds wiring s2, and it is a standard cell SC 12. It connected. Primitive cell train GC 1 which replaced with the standard cell SC 4 in circuit modification in the 4th example, and was arranged by the free area 16 Standard cell SC 11 It connects through wiring s3 and is the primitive cell train GC 1. Standard cell SC 12 It connected through wiring s4 and the wiring s1 and s2 shown in drawing 10 is deleted. Moreover, primitive cell train GC 1 arranged by the free area 16 The high order power-source wiring (VDD) 17 is connected to the high order power-source wiring 11 of cel line 15b through wiring 18, and it is the primitive cell train GC 1. The lower order power-source wiring (VSS) 19 is connected to the lower order power-source wiring 12 of cel line 15a through wiring 20.

[0036] Furthermore, in circuit modification shown in drawing 10 , the standard cell SC 3 of cel line 15c minds wiring s5, and it is a standard cell SC 13. It connects and is a standard cell SC 13. It connected with the standard cell SC 2 through wiring s6. As the 4th example shows to drawing 11 on the other hand, it is a standard cell SC 13. Two primitive cell GC2 which replaced with and was arranged by cel line 15b It uses. That is, at drawing 11 , it is primitive cell GC2. A standard cell SC 3 is connected through wiring s7, and it is primitive cell GC2. The standard cell SC 2 was connected through wiring s8, and wiring s5 and s6 is deleted. Moreover, the standard cell SC 4 of cel train 15b used no longer and the standard cell SC of cel train 15c 13 The wiring layer is deleted.

[0037] According to the gestalt of operation of the 1st of this invention, it becomes possible to correct a circuit only by modification of wiring, and circuit modification can be carried out for easy and a short period of time so that clearly also from the 3rd and 4th examples. Moreover, it can constitute semi custom-made ASIC on the same semiconductor chip, using the standard cell and primitive cell which were shown in the 3rd and 4th examples two or more.

[0038] The 5th example drawing 12 is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the 5th example of the gestalt of operation of the 1st of this invention.

[0039] In drawing 12 , wiring grid 26x-26y is formed on the field of the primitive cell (field shown with the slash upward slanting to the right surrounded by the thick wire) 25 of the standard cell 23 (field shown with the slash of the Hidari riser surrounded by the thick wire) arranged at the cel lines 21 and 22, and the gate array arranged at the free area 24. The place by which it is characterized [of the 5th example] has the track group x1 of a lengthwise direction, x2, --, wiring with which this track group top was set for x21 and -- to width of face among wiring grid 26x-26y in having adjusted the physical relationship of the lengthwise direction of a standard cell 23 and a primitive cell 25 so that a level difference might not arise in the cel line 21, a free area 24, and the cel line 22 and it could pass. The lateral track group y1 and y2 Of course about y15 and --, height is unified [-- and] like the 2nd - the 4th example. That is, in the integrated circuit of the hybrid standard cell concerning the 5th example of the gestalt of operation of the 1st of this invention, the standard cell 23 and the primitive cell 25 are arranged according to the same wiring grid system 26x-26y.

[0040] If it is in such 5th example, wiring of the gate array on the free area 24 of cel spacing can be easily performed along with wiring grid 26x-26y. Furthermore, if the dimension (height H and width of face WG) of the primitive cell 25 of a gate array is designed for the dimension (height H and width of face W1, W2, W3, --) of a standard cell 23 as a base unit, the constraint on arrangement / wiring will be eased further, and both mixed loading will become very easy. It is the width of face WG of the primitive cell 25 of a gate array about operation W1, for example, the width of face of a standard cell 23, W2, W3,

and --. The 6th [to design so that it may become one n times (n= 1, 2 and 3 --) the integer of this] example drawing 13 is the 6th example which applied the gestalt of operation of the 1st of this invention to the array of a channel loess form standard cell. That is, it is the structure which has arranged primitive cell GC of a gate array to the free area 33 on the array pattern of standard cells SC11, SC12, SC21, SC22, SC31, SC41, and SC42. Since a degree of integration improves by covering the whole surface with a standard cell as a channel loess form, and there is no fixed wiring field and the design of wiring has primitive cell GC of a gate array on the outskirts in addition to an easy advantage, modification of a circuit becomes very easy. According to the wiring grid x1 with same standard cells SC11, SC12, SC21, SC22, SC31, SC41, and SC42 and primitive cell GC of a gate array, x2, --x30, --;y1, y2, --y27 --, it is arranged like the 5th example.

[0041] Drawing 14 shows the flat-surface layout at the time of forming a metal wiring layer on it to the lower layer pattern shown in drawing 13 using the wiring grid x1, x2, --x30, --;y1, y2, --y27 --. As shown in drawing 14 , the high order power-source wiring (VDD) 11 and the lower order power-source wiring (VSS) 12 are arranged as power-source wiring respectively common to the cel train of the upper and lower sides in the boundary section of an upper cel train and a lower cel train. The high order power-source wiring (VDD) 11, lower order power-source wiring (VSS) 12 and the horizontal wiring 501, 502, --, 516 constitute the 1st-layer metal wiring. The horizontal wiring 401, 402, --, 415 is the 2nd-layer metal wiring, and the vertical wiring 601, 602, --, 613 is the 3rd-layer metal wiring. Moreover, these 1st-layer metal wiring and standard cells, or connection with the primitive cell of a gate array, The 2nd-layer metal wiring, a standard cell, or connection with the primitive cell of a gate array, The 1st layer and 2nd-layer connection between metal wiring, the 2nd layer and 3rd-layer connection between metal wiring, etc. are made through the contact holes (or veer hole) 701, 702, --, 737 prepared into each interlayer insulation film prepared the bottom of these wiring, or between them. In addition, drawing 14 is an example and, of course, you may have the metal wiring layer of the 4th more than layer further.

[0042] [Gestalt of the 2nd operation] drawing 15 is drawing showing the configuration of the whole chip of the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 2nd of this invention. The gestalt of operation of the 2nd of this invention starts a large-scale circuit system. That is, since memory, a core based CPU, ALU, A/D, a D/A converter, and various I/O circuits also including a display are included in a circuit system with the latest large-scale LSI for multimedia etc., the gestalt of operation of the 2nd of this invention explains the example of a configuration at the time of carrying such a subsystem on one LSI chip. Specifically, LSI which loaded together the megger function 211,212 and the logical circuit fields (logical circuit block) 231, such as a mega cell 213 and ALUs, such as ROM and RAM, and a core based CPU, on the same semiconductor chip is explained.

[0043] The logical circuit block on LSI chip 1 shown in drawing 15 arranges primitive cell GC of a gate array to the free area of a standard cell SC on the basis of a channel loess form standard cell. In this en BEDDEDDO array, although pattern arrangement of the similar mixed-loading mold LSI chip called an en BEDDEDDO array (embeded array) was known conventionally, the primitive cell of a gate array, or when it was altogether covered with the standard cell and circuit modification arose, all logical circuit blocks needed to redo lower layer pattern modification, an ion grouting degree, etc., and a design and production time of long duration were required for them.

[0044] With the gestalt of operation of the 2nd of this invention, as shown in drawing 15 , primitive cell GC of a gate array is preparatorily arranged to the free area by which the standard cell SC in a logical block 231 is not arranged, various circuit modification is attained only by modification of wiring, without affecting the circuitry of a standard cell, since it is made to make a circuit change using this primitive cell GC, and a development cycle can be shortened. Moreover, by doubling so that the specification of a standard cell SC and primitive cell GC can be arranged on the same grid, both mixed loading can be made easy and the constraint on arrangement wiring can be sharply eased compared with the former.

[0045] Since the size of a transistor is immobilization, the primitive cell of a gate array has the fault which is not made even if he wants to make a transistor small depending on a specification and to make power consumption small. On the other hand, since the size of a transistor will be adjustable within the

cel even if height H of a cel is immobilization, a standard cell can make size of a transistor small according to requirement specification, and can lower power consumption. According to the gestalt of operation of the 2nd of this invention, since the primitive cell and standard cell of a gate array are appropriately combinable, it is possible to lower the power consumption of the whole LSI chip. Moreover, it is the same as that of the gestalt of the 1st operation that arrangement of the middle buffer for controlling increase and the clock skew of drive capacity with the combination of a standard cell and the primitive cell of a gate array becomes easy.

[0046] Of course in the gestalt of operation of the 2nd of this invention, structure with the wiring channel field explained with the gestalt of the 1st operation may be adopted as a pattern in a logical block 231. In addition, of course, the structure of the 1st explained with the gestalt of the 1st operation - the 6th example is also applicable.

[0047] The gross area which the gross area which the standard cell SC in a logical block 231 occupies, and primitive cell GC of a gate array occupy may have large whichever. What is necessary is just to choose the ratio of a gross area with a circuit specification.

[0048]

[Effect of the Invention] According to this invention, when specification modification of an integrated circuit and a design change arise, a circuit change can be made, without affecting the circuitry of a standard cell. That is, it is not necessary to redo a lower layer ion grouting degree etc., various circuit modification is attained only by modification of the upper wiring, and the development cycle of an integrated circuit can be shortened.

[0049] Moreover, according to this invention, the constraint on both arrangement wiring can be sharply eased compared with the former by doubling the base dimension of a standard cell and a primitive cell, or arranging these cels on the same grid.

[0050] Furthermore, according to this invention, it is possible to lower the power consumption of the whole LSI chip by combining the primitive cell and standard cell of a gate array appropriately. That is, high integration and low-power-izing of a standard cell become possible [combining both the features that it is easy and a circuit design is rich in flexibility, and the features that the development cycle of a gate array is short] by loading together a standard cell and the primitive cell of a gate array to a logical circuit field (logical block).

[0051] Furthermore, according to this invention, according to this invention, an improvement of properties, such as the operation time of a large-scale LSI chip and power consumption, and the formation of a high accumulation consistency are easy for the pan with which arrangement of the middle buffer for controlling increase and the clock skew of drive capacity with the combination of a standard cell and the primitive cell of a gate array becomes easy, and, moreover, the flexible circuit design of them becomes possible at it. And it can respond promptly also to a design change and TAT becomes short.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 1st of this invention.
[Drawing 2] It is drawing showing other configurations of the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 1st of this invention.
[Drawing 3] It is drawing showing the configuration of further others of the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 1st of this invention.
[Drawing 4] It is drawing showing the configuration of further others of the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 1st of this invention.
[Drawing 5] It is drawing showing the configuration in the case of arranging the middle buffer for controlling clock skew in the integrated circuit of the hybrid standard cell concerning the gestalt of operation of the 1st of this invention.
[Drawing 6] It is drawing showing the lower layer pattern of the integrated circuit of the hybrid standard cell concerning the 1st example of the gestalt of operation of the 1st of this invention.
[Drawing 7] It is drawing in which the upper wiring layer was formed on the pattern of drawing 6 .
[Drawing 8] It is the equal circuit of drawing 7 .
[Drawing 9] It is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the 2nd example of the gestalt of operation of the 1st of this invention.
[Drawing 10] It is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the 3rd example of the gestalt of operation of the 1st of this invention.
[Drawing 11] It is drawing showing the example which made a circuit change to the circuitry which starts the 4th example of the gestalt of operation of the 1st of this invention, and is shown in drawing 10 .
[Drawing 12] It is drawing showing the configuration of the integrated circuit of the hybrid standard cell concerning the 5th example of the gestalt of operation of the 1st of this invention.
[Drawing 13] It is drawing showing the pattern which was applied to the 6th example of the gestalt of operation of the 1st of this invention, and has arranged the primitive cell of a gate array to the free area of a channel loess form standard cell.
[Drawing 14] the drawing 13 top -- the 1- it is drawing showing the example which has arranged the 3rd-layer metal wiring.
[Drawing 15] It is the mimetic diagram showing the pattern arrangement at the time of starting the gestalt of operation of the 2nd of this invention, and carrying a mega cell, a megger function, and a standard cell gate array mixed-loading form logical block on the same chip.
[Drawing 16] It is drawing showing the configuration of the whole integrated circuit chip of the conventional standard cell.
[Drawing 17] It is drawing showing the configuration of the whole chip of the conventional en BEDDEDDO array (embeded array).
[Description of Notations]

1 Chip
2, 5, SC1 and SC2, --, SC5, SC11, SC12, SC13, SC11, SC12, SC21, SC22, SC31, SC41, SC42 Standard cell
3, 14a, 14b, 16, 24, 33 Free area
4, 6, GC Primitive cell of a gate array
9, 11, 17 High order power-source wiring (VDD)
10, 12, 19 Lower order power-source wiring (VSS)
13, 15, 21, 22 Cel line
18, 20, s1, s2, --, s8 Wiring
26x-26y Wiring grid
51 Clock Driver
52, 53, --, 58 Middle buffer
61, 62, 63, 64 Gate polish recon
71S, 75S p+ source field
71D, 75D p+ drain field
72S, 76S n+ source field
72D, 76D n+ drain field
73 77 n+ source field
74 78 p+ contact field
95 97 p well
96 98 n well
211,212 Megger function
213 Mega Cell
231 Logical Circuit Field (Logical Circuit Block)
501, 502, --, 516 Horizontal wiring
601, 602, --, 613 Vertical wiring
701, 702, --, 737 Contact hole (or veer hole)

[Translation done.]

* NOTICES *

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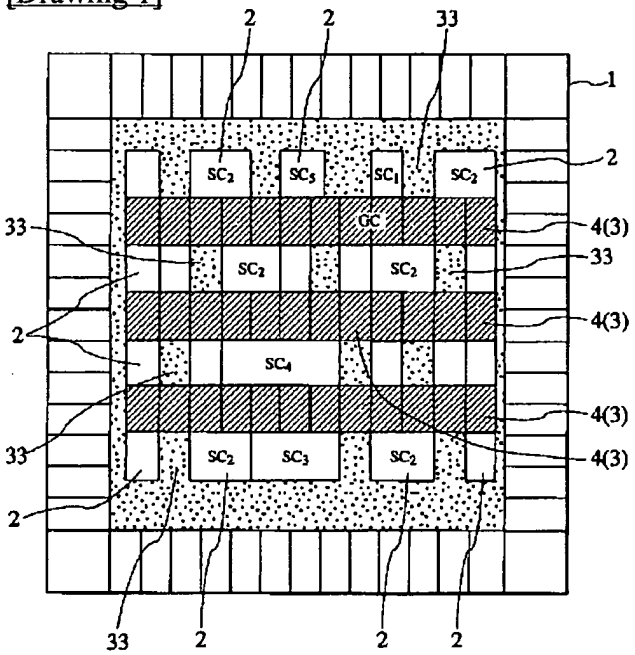
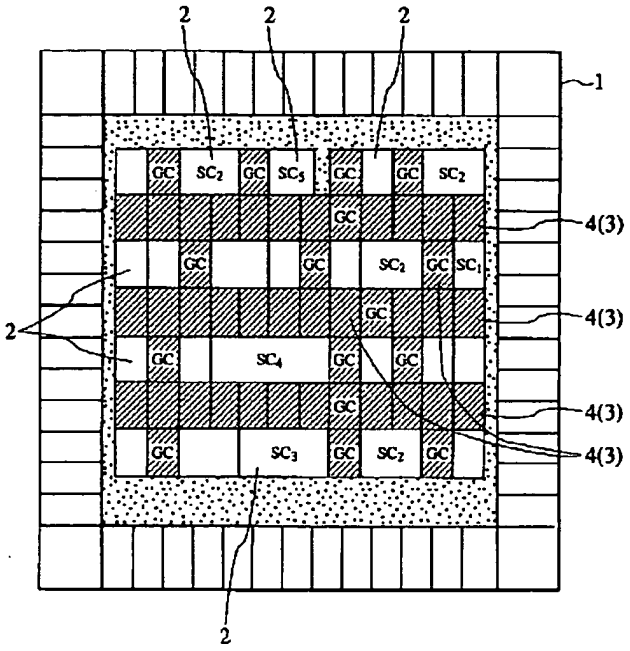
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

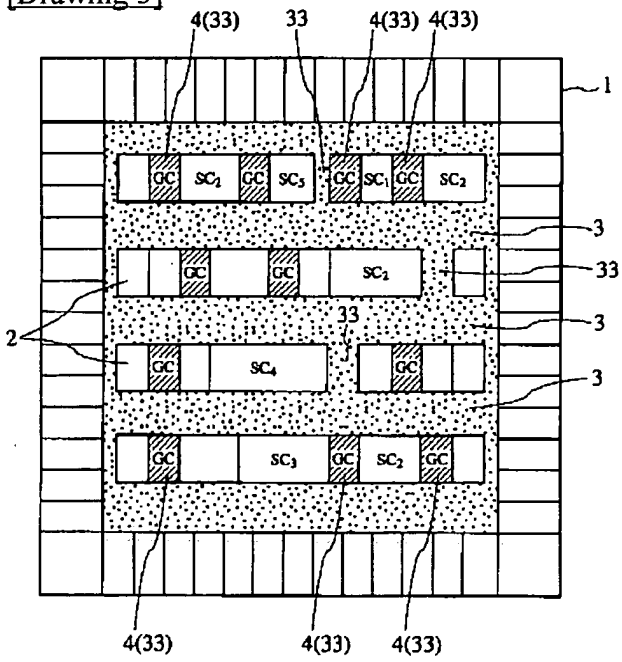
[Drawing 1]



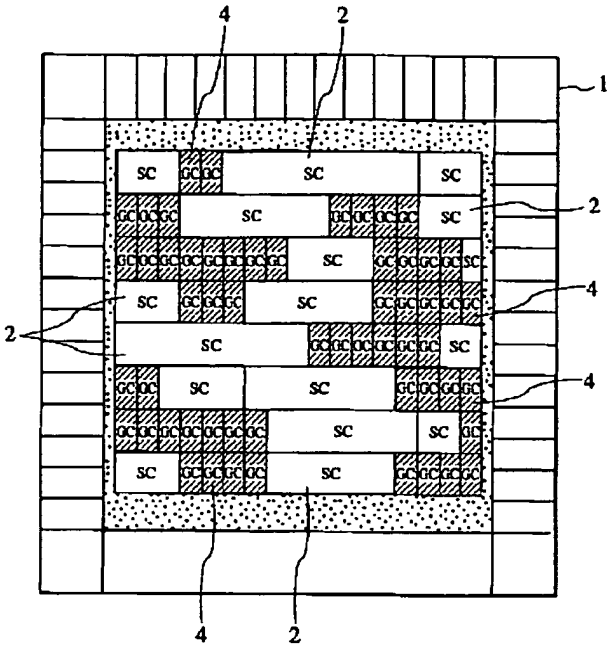
[Drawing 2]



[Drawing 3]



[Drawing 4]



[Drawing 5]

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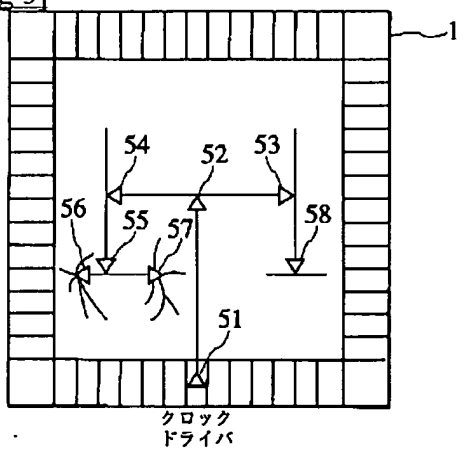

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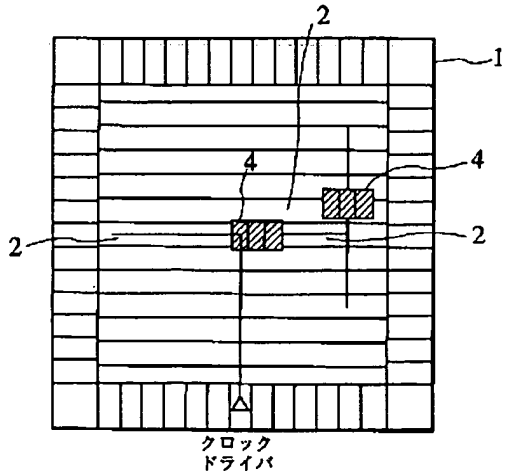
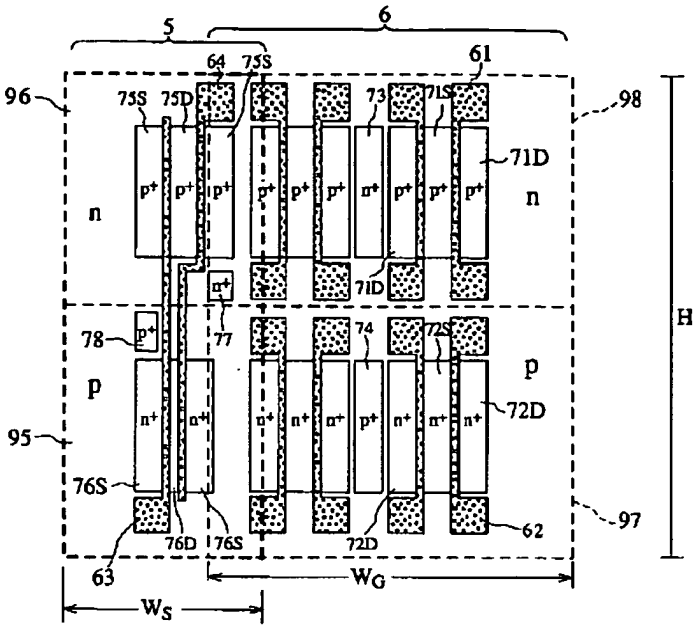
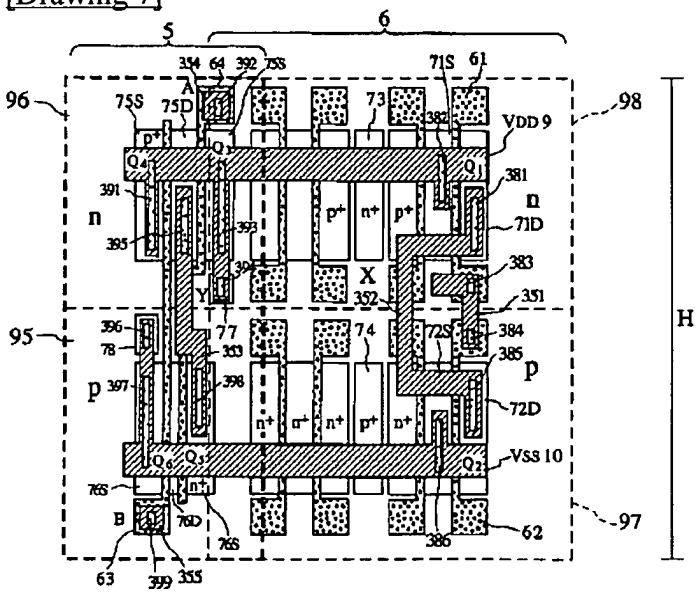


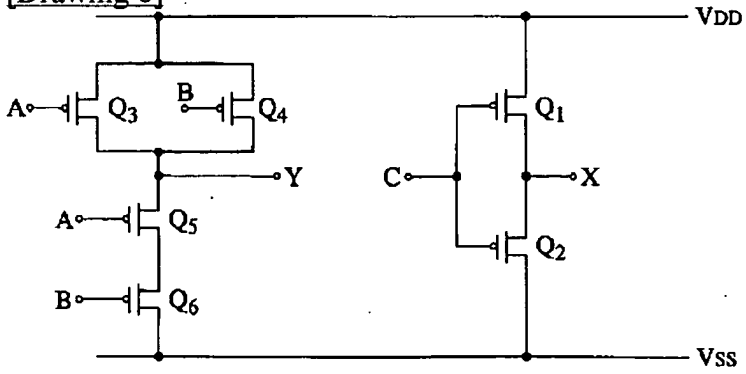
[Drawing 6]



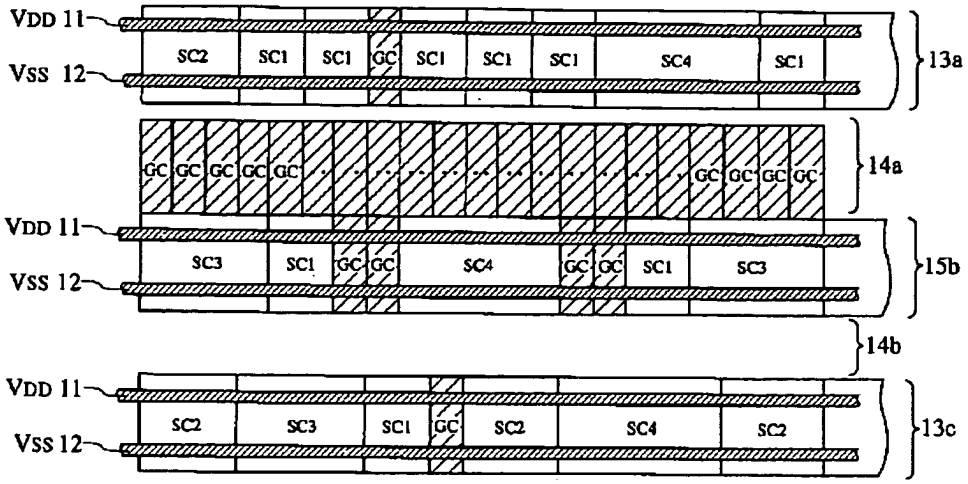
[Drawing 7]



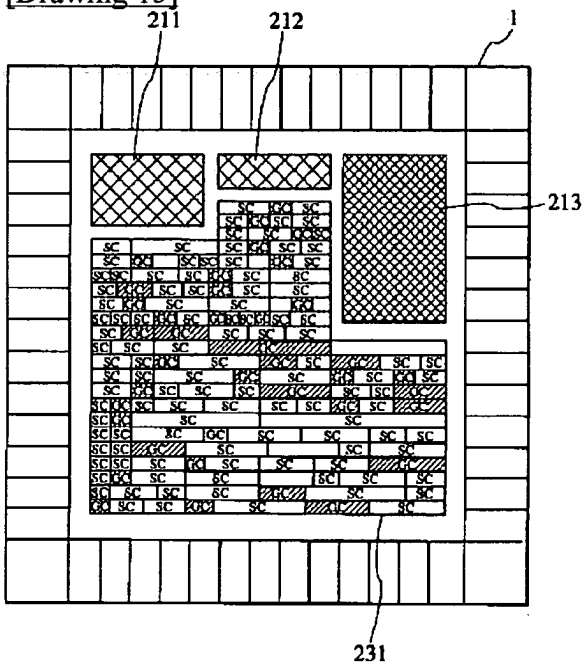
[Drawing 8]



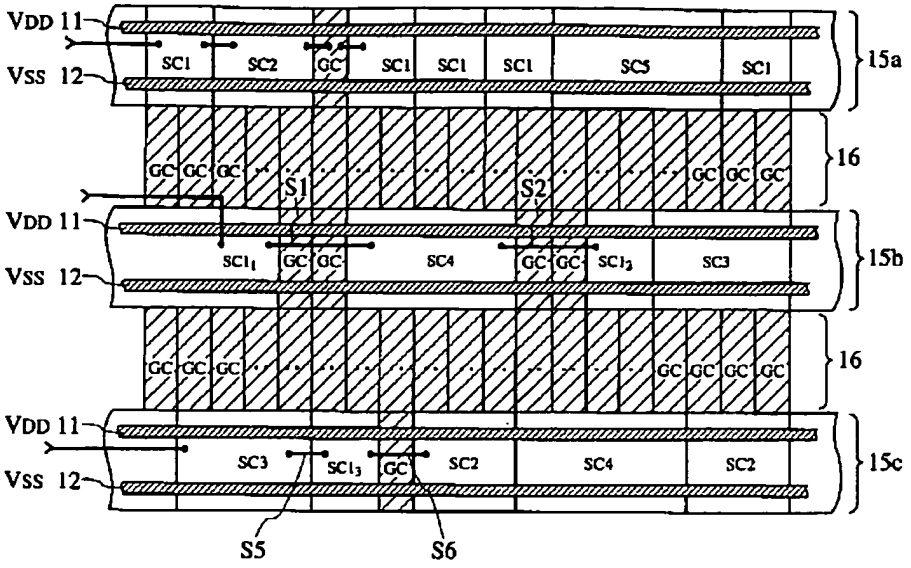
[Drawing 9]



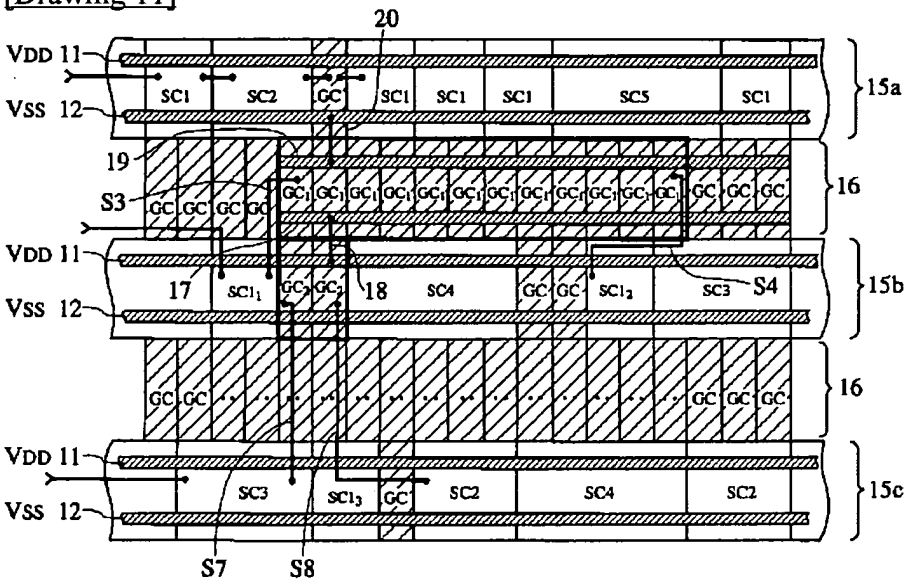
[Drawing 15]



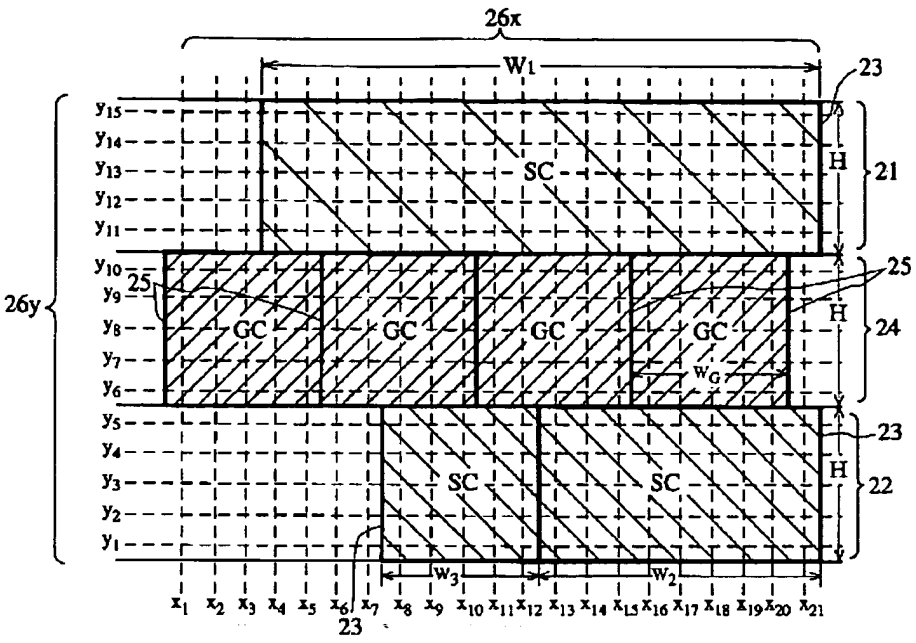
[Drawing 10]



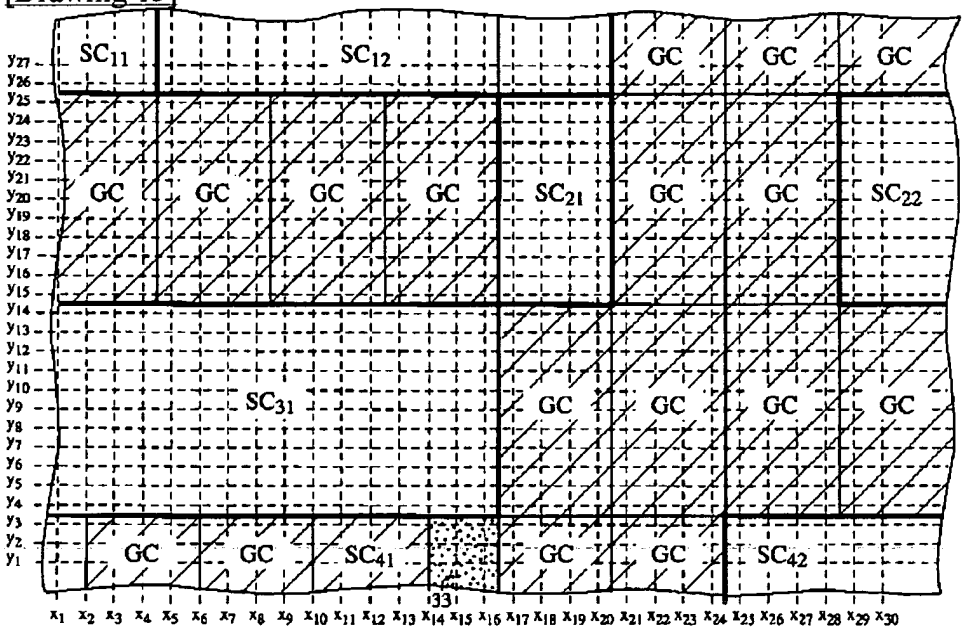
[Drawing 11]



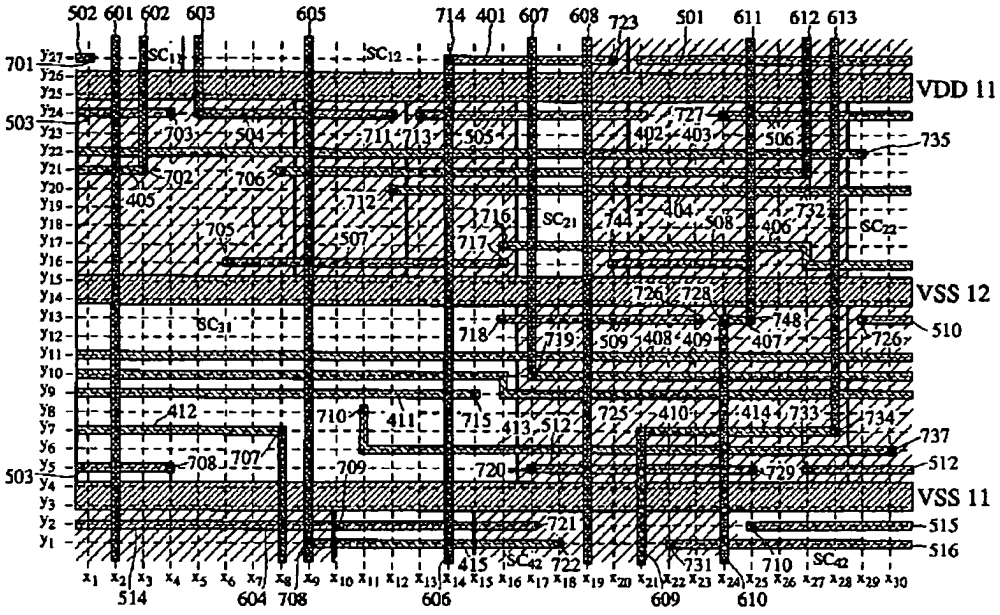
[Drawing 12]



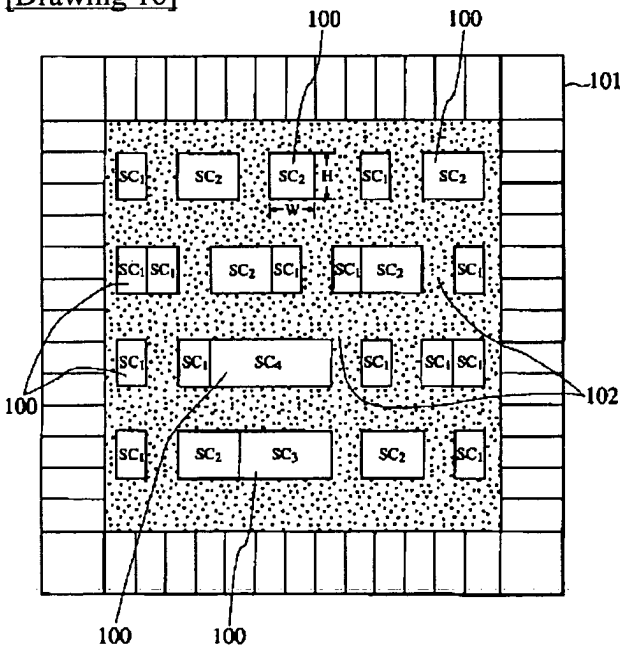
[Drawing 13]



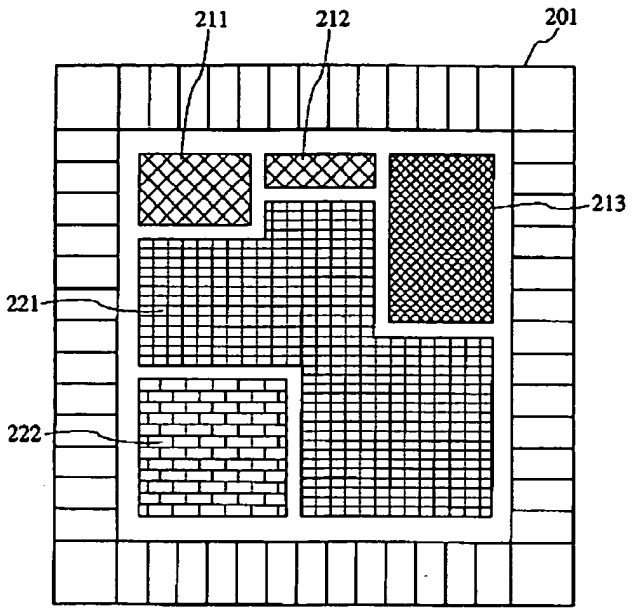
[Drawing 14]



[Drawing 16]



[Drawing 17]



[Translation done.]